IN THE CLAIMS

Please add claim 18 as indicated below.

The listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claim 1 (previously presented) A method of providing a semiconductor device, the semiconductor device including a first layer desired to be etched, the method comprising the steps of:

(a) providing an antireflective coating (ARC) layer having antireflective properties, wherein the ARC layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer;

(c) etching the first portion of the first layer;

(d) removing the resist layer utilizing a plasma etch, the ARC layer being resistant to the plasma etch;

(e) patterning a second resist layer, the second resist layer including a pattern having a plurality of apertures therein for etching a second portion of the first layer; and

(f) etching the second portion of the first layer.

Claim 2 (original) The method of claim 1 wherein the ARC layer providing step (a) further includes the steps of:

(a1) depositing the ARC layer.

Claim 3 (previously presented) The method of claim 1 wherein the resist layer removing step (d) further includes the step of:

(d1) performing the plasma etch using a plasma including a forming gas, the ARC layer being resistant to the plasma etch using the plasma including the forming gas.

Claim 4 (original) The method of claim 3 wherein the plasma further includes four percent of the forming gas.

Claim 5 (previously presented) The method of claim 3 further comprising the step of:

(d2) providing a wet preclean after the plasma etching step (d1).

Claim 6 (original) The method of claim 1 wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent.

Claims 7 – 12 (cancelled)

Claim 13 (previously presented) A method of providing a semiconductor device including first and second regions having, respectively, first and second types of circuit structures, the method comprising:

depositing a first layer on a substrate;

depositing a layer of SiON on the first layer;

depositing a first resist layer on the SiON layer;

patterning the first resist layer for etching the first layer in the first region of the semiconductor device;

etching the first layer in the first region of the semiconductor device;

removing the first resist layer utilizing a plasma etch;

depositing a second resist layer on the SiON layer;

patterning the second resist layer for etching the first layer in the second region of the semiconductor device;

etching the first layer in the second region of the semiconductor device;

removing the second resist layer; and

removing the SiON layer.

Claim 14 (previously presented) The method of claim 13 wherein the SiON layer has a thickness of less than about 500 Angstroms.

Claim 15 (previously presented) The method of claim 13 wherein the SiON layer has a thickness of about 300 Angstroms.

Claim 16 (previously presented) The method of claim 15 wherein the SiON layer has a thickness of between about 270 and about 300 Angstroms.

Claim 17 (previously presented) The method of claim 13 wherein the first type of circuit structure comprises structures for forming memory cells and the second type of circuit structure comprises structures for forming logic circuits.

Claim 18 (new) A method for reducing antireflective coating (ARC) layer removal comprising the steps of:

depositing an ARC layer on a first layer, wherein said ARC layer comprises a layer of SiON having a thickness of less than 500 Angstroms (Å);

patterning a first resist layer on said ARC layer, wherein said first resist layer comprises a pattern having a plurality of apertures therein for etching a first portion of said first layer;

etching said first portion of said first layer;

removing said first resist layer utilizing a plasma etch after said first portion of said first layer is etched, wherein said ARC layer is resistant to said plasma etch;

patterning a second resist layer, wherein said second resist layer comprises a pattern having a plurality of apertures therein for etching a second portion of said first layer; and

etching said second portion of said first layer.